FIDES-P1 AC – DC Power Device

AC DIRECT LED DRIVER

PRELIMINARY BRIEF DATA

The FIDES free voltage AC to DC LED driver using patented Yeonmoon Jeong Adaptive AC phase currents to voltages with zero currents valley fill power device are smart LED power driving chipset for supports all the attractive features of ECO LED lighting products such as high efficiency 95% over with excellent PFC 0.95, ultra small package, low cost, design flexibility, and easy design-in, these parts are targeted to more sophisticated applications and offer several enhanced technology and features, including continuous AC and DC both of input voltage coverage from 10-300V wide ranges and output load up to 5 to 100Watts without aluminum electrolytic capacitor and transformer.

The isolation power and non-isolation power for LED switch transistors are external of main chipset for supports design free are no requires reducing power consumption of the constituent devices such as multi output power provide redundancy.

Also included built-in features likes thermal sensor, direct connection to external ambient sensor is automatic LED brightness control self thermal controller and PLC communication makes smart grid network.

The employed phase current detection technology is automatically current error corrections for each LED load current transition. This phase current driving technology is compensation to regulated AC input with LED loads to independently protection for over power and open or short circuits protection with over-temperature controls.

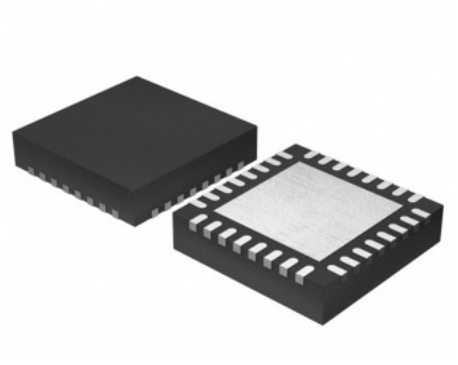
These features simplify the task of the LED monitor back light or LED bulb and QFN36 small package are supports the smart fixture design and allow for the use for lower-end Factories.

FEATURES

- Free input AC10~300V Range
- Un regulated DC input
- Up to 3 LED group in series
- Dimming support : Thermal surveillance to extend LED life time, Day and night luminance Power Configurable
- Direct connect illumination driver Installed
- 125°C shutdown and selectable Temperature(60°~125°) synchronized controller embed
- On/Off and Dimming by PLC modem to seamless attachable option (SPI)
- -40°C ~ +85°C

TYPICAL APPLICATIONS

- LED TV, Monitor, High power LED lighting
- Etc

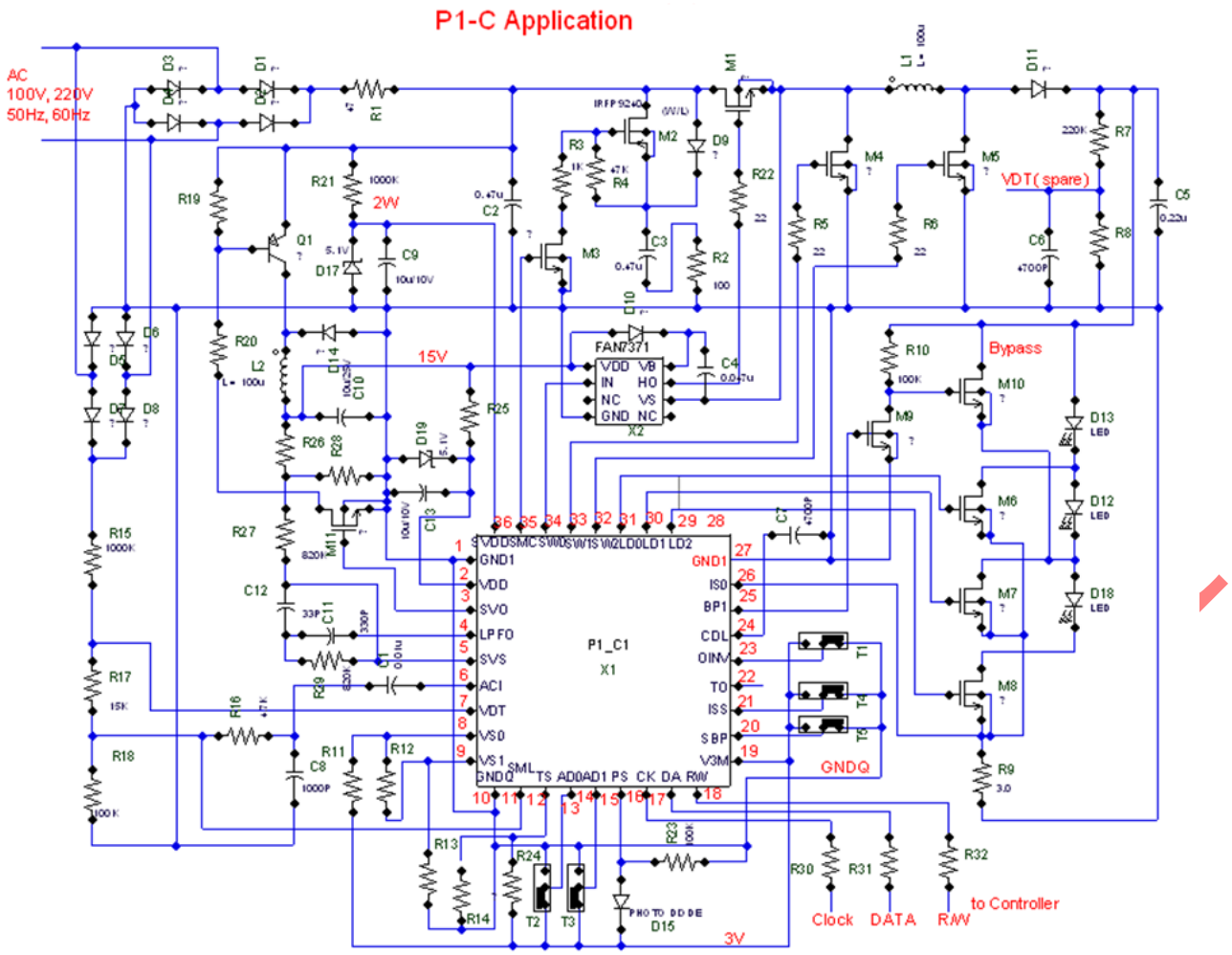


4Metal 2Poly(27layer) 0.35uM CMOS Process

FIDES-P1 QFN-36 Engineering sample (6mmX6mm)

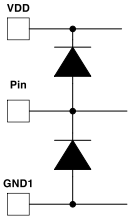
CV,CC accurate PWM modulation for constant current by supplied voltaic driving it ideal for configuration to multiple LED applications.

Typical Application Circuit

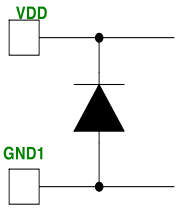
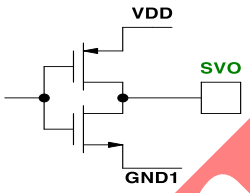
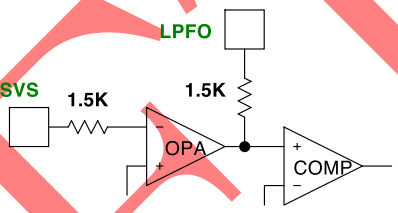
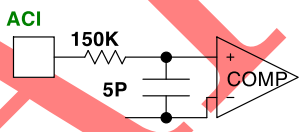
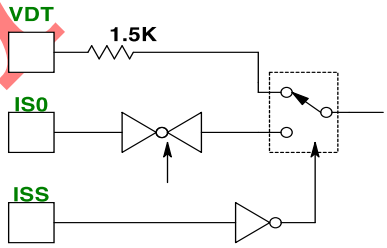
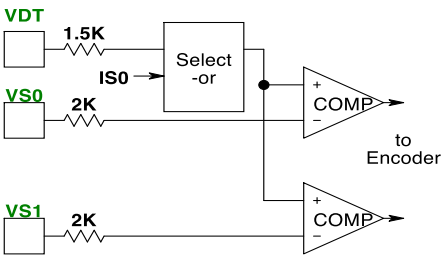


Terminal descriptions

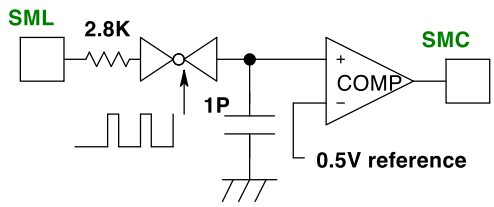
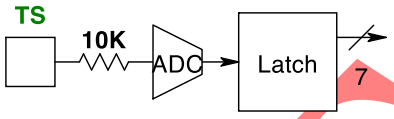
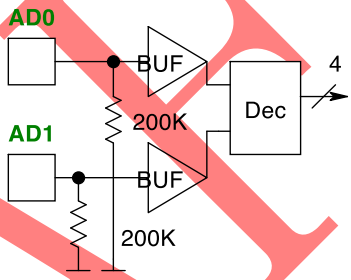
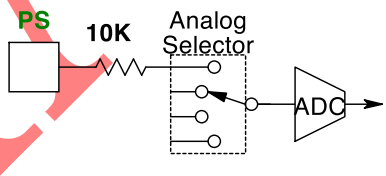
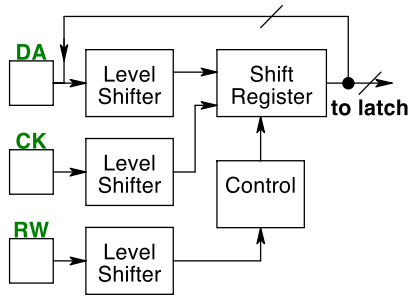
IO: I=input, O=output, B=Bidirectional, - = no connection

Pin #	Pin Name	Description	Circuit (shows Input or output port)	Voltage
	General	Every pins except ground and power supply pins have ESD (Electrical static damage) protection diodes between pin and ground and VDD potential.		
1	GND1	Ground for large current. Connect to near minus port of bridge rectifier diode.	(Bi-directional)	5V

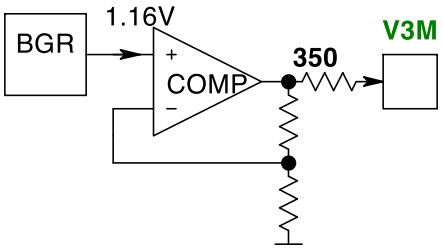
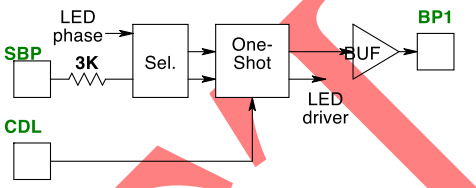
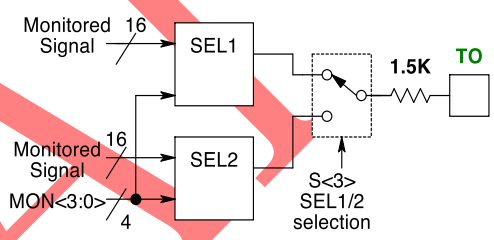
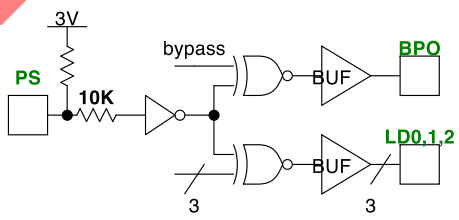
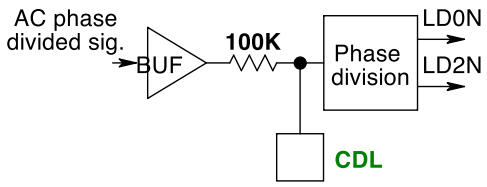
jeong.osc@gmail.com

2	VDD	Power Supply for chip 5 +/- 0.5V		0V
3	SVO	PWM output for Sub-regulator The NMOS load is needed.	(Logic Output) 	**0 – 5V**
4	LPFO	Low pass filter output for Sub-regulator Load impedance: >100Kohm	(Analog Output), (Analog Input) 	0.3 – 4.5V
5	SVS	Low pass filter input for sub-regulator. Lag-lead LPF can be available to connect capacitors and resistors externally between SVS and LPFO.		1.16V
6	ACI	Full wave AC signal input. Vin= 1 to 2Vpp. PC pattern layout has to be paid attention in order to avoid noise injection through PC pattern.	(Analog Input) 	1.66V
7	VDT	AC signal input for multi-phase generation. This pin is valid while ISS pin is set to zero level. (The AC signal has to be detected before rectifier)	(Analog Input) 	- (Hi-Z)
8	VS0	Reference voltages for AC phase angle generation. VS0: high side of reference voltage VS1: low side of reference voltage	(Analog Input) 	-
9	VS1			Hi-Z
10	GNDQ	Quiet ground for mainly analog circuit. The potential of this ground should be higher than GND1.		o
11	SML	Voltage setup for quick charge level.	(Analog Input)	

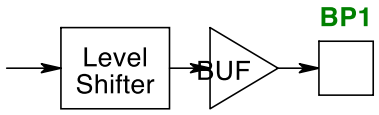
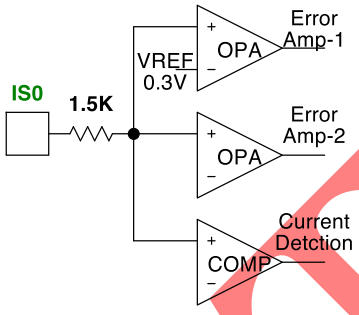
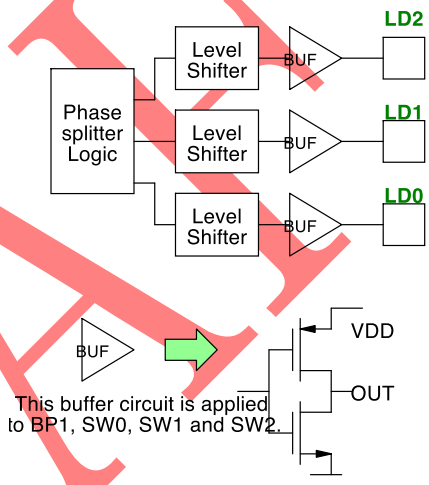
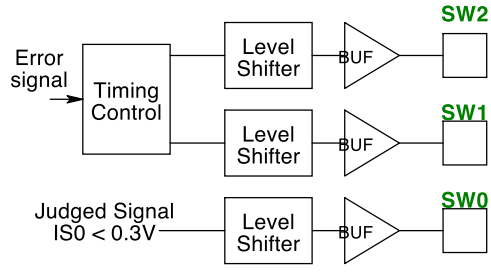
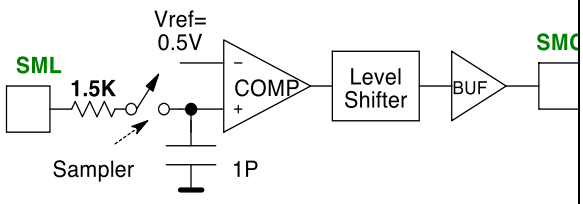
jeong.osc@gmail.com

		Internal reference voltage=0.5V. The input voltage must not exceed 3V in every condition.		- Hi-Z
12	TS	Temperature detection starts level setup. The DC level of this pin can select following temperature level setup; 60C=0.188V, 65C=0.563V, 70C=0.938V, 75C=1.313V, 80C=1.688V, 85C=2.063V. The accuracy of external voltage setup resistors have to be within +/-2%.	(Analog Input) 	- Hi-Z
13 14	AD0 AD1	Chip selection for serial register data transmission. The combinations are; (AD0,AD1)=(0,0), (0,1), (1,0) or (1,1) With 200Kohm Pull-down resistors	(Logic Input) 	0V
15	PS	Photo sensor input 0V= maximum brightness of LED 2.4V=turns LED off Continuous brightness control can be available between 0V and 2.4V.	(Analog Input) 	- Hi-Z
16	CK	Serial Clock input for external control	(Logic Input and Output) 	Hi-Z
17	DA	Serial Data IO from external control		Hi-Z
18	RW	Serial data Read or Write selection Logic level =0 – 5V		- Hi-Z
19	V3M	Regulated 3V output I-output <500uA	(Analog Output)	3.0V

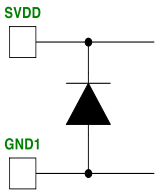
jeong.osc@gmail.com

				
20	SBP	Bypassing a LED or two LEDs 0=All LEDs available, 1=Bypass LEDs.	(Logic input) 	- Hi-Z
21	ISS	AC phase generator source selection 0=VDT input, 1=ISo input	(Logic Input) Refer to VDT (pin 7)	- Hi-Z
22	TO	Internal status monitor output The monitored signals are selected by MON<3:0> which data is set up by serial data. The 1 by 16 selectors, SEL1 and SEL2, are selected by S<3> switch. Refer to table-1 for monitored signals	(Analog Output) 	Open at default Depending on register setup
23	OINV	The polarity of output of LED drive pins, LDo, LD1 and LD2, 0=normal polarity 1=reversed polarity This is used when LED drive FETs are needed to be inverted twice.	(Logic Input) 	3V
24	CDL	Timing capacitor to generate pulse width of LDo division. Around a 100pF externally connected capacitor recommended	(analog Input) 	0 – 3V
25	BP1	LED Bypassing control signal output Active low output.	(Logic output)	0 – 5V

jeong.osc@gmail.com

		An NFT or a NPN BJT is needed for a load.		
26	ISo	LED current sense input. A register, Rs, has to be connected between ISo pin and ground externally. The resistance can be calculated as; Rs=0.3/I_LED (I_LED=LED current) Ex) if I_LED=100mA, then Rs=3 ohms.	(Analog Input) 	- Hi-Z
27	GND1	Ground. Same as GND1.	See GND1 and VDD.	oV
28		not used		
29	LD2	LED2 driver output. External power NMOS needed. Turns on at top voltage of AC.		o - 5V
30	LD1	LED1 driver output. External power NMOS needed. Turns on at middle voltage of AC.		
31	LDo	LEDo driver output. External power NMOS needed. Turns on at lower voltage of AC.		
32	SW2	Voltage boosting output. Power NMOS is needed externally.	(Logic Output) 	o - 5V
33	SW1	Buck switcher. External Power NMOS is needed externally.		
34	Swo	Voltage switcher. High-side Gate driver chip needed externally		
35	SMC	Quick discharge driver output. Charged voltage to the external capacitor by AC rectified wave (ripple) is discharged at certain ripple level which is defined at DC level of SML (pin 11).	(Logic Output) 	o – 5V

jeong.osc@gmail.com

36	SVDD	Sub-regulator power supply SVDD=5.0+/-0.5V		5.0V

jeong.osc@gmail.com

Item	Symbol	Parameter	min	typ	max	unit	Condition
Rated Voltage Range	VDD		4.5	5.0	5.5	V	Max V =6.0V
Junction Temperature	Tj		-40	25	125	℃	
Logic Low input V	ViL	AD0, AD1,ISS, SBP, RW, CK, DA, REGSEL, OINV	0		0.2VREF	V	
Logic High input V	ViH		0.8VREF		VREF	V	
Logic Low output V	VoL	DA Terminal	0		0.2VREF	V	
Logic High output V	VoH		0.8VREF		VREF	V	
Low Level output I	IoL				-1	mA	
High Level output I	IoH		1			mA	
Switch Clock Freq	FCLK			200		KHz	
Dimmer range	DIM		1		255		
Drive current	I_DRV	LD0-2、 SW0,1,2,3 Terminal	40			mA	
Regulator output	VREF	VREFO Terminal	2.95	3.0	3.05	V	
Max AC V detect	V_AC	VDT Terminal	0		VDD	V	
LEDV divide	V_LEDD	VS0, VS1	0.1		VDD	V	
Ambient detect	VL	PS Terminal	0.15		1.5	V	
LEDcurrent Threshold	VTHIS	IS0 Terminal				V	Comparate with saw
Power consumption					5	mA	

Table 1

Monitored signal selection (Output at "TO")

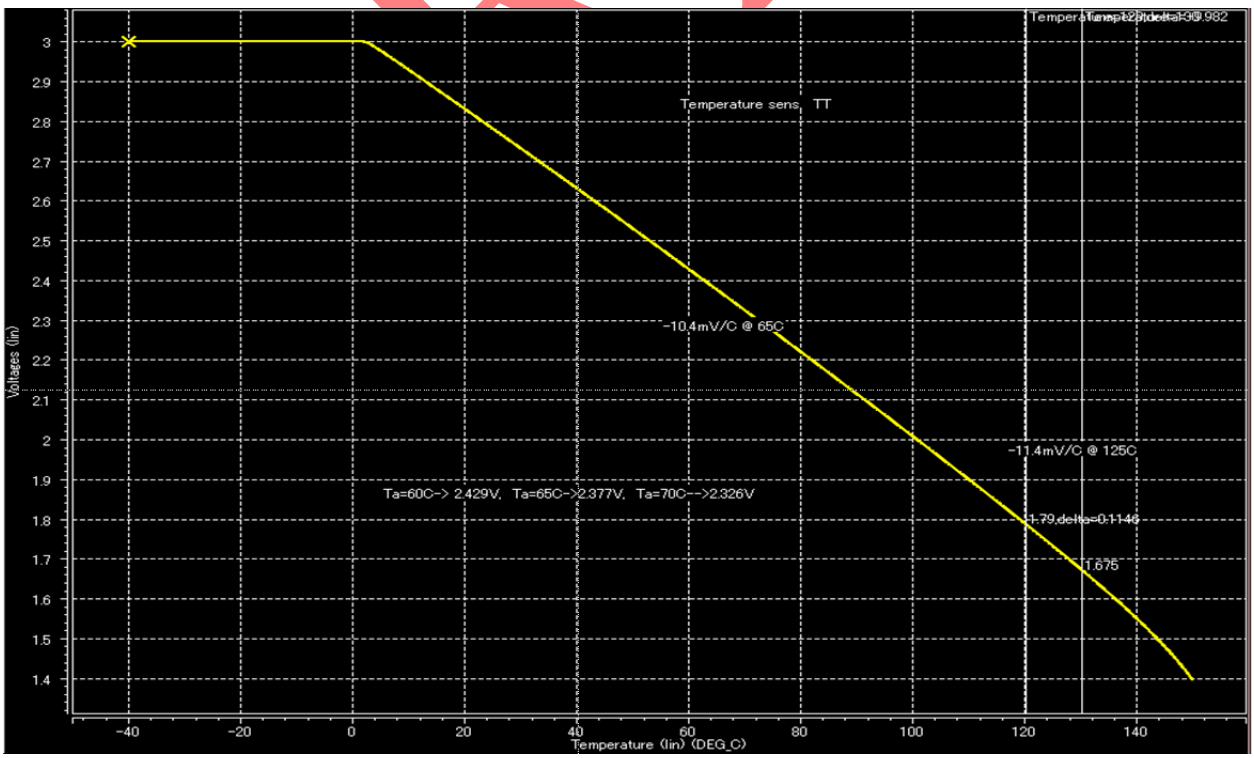
#	MON <3:0>	TO S<3>=0	Voltage	TO S<3>=1	Volt -age
0	0000	Open	-	Open	-
1	0001	GNDQ (quiet Ground)	0	GNDQ (quiet Ground)	0
2	0010	BGRO(Band Gap Regulator) output	1.16V	RNX(Power On reset output)	0

jeong.osc@gmail.com

3	0011	V3Q (Quiet 3V)	3V	V3N (Noisy 3V)	3V
4	0100	VHA (ADC6 Reference High Voltage)	2.43V	VLA(ADC6 Reference Low Voltage)	1.7V
5	0101	ADTA (Temperature voltage for ADC)	3V	TAO (Temperature Sense Voltage)	1.85V
6	0110	GNDQ (quiet Ground)	0	GNDQ (quiet Ground)	0
7	0111	VSWO (Saw Tooth wave of main reg)	2V	ISOOO (LED Current Sense Buffer Voltage)	0.3V
8	1000	CK39 (Around 39Hz output)	Pulse	ILMLO (ISOOO & 0.12V Comparator Output)	0
9	1001	CK78 (Twice Frequency of CK39)	Pulse	CK10K (10KHz clock output)	Pulse
10	1010	CKMON (Clock Signal)	Pulse	DMO (Dimmer Pulse output)	Pulse
11	1011	ISRPO (Error Amp Comparator Output)	0	LSRPO (Error Amp ILM Output)	Pulse
12	1100	ACZ (AC zero Cross Output)	Pulse	ACPLS –Not used	
13	1101	MODU (DUEN (Up/Down) Output)	Pulse	MOMCK (Sub –reg clock output)	Pulse
14	1110	SHTDWN (Shut Down at Tj>125C)	0	Open	
15	1111	Open		Open	

Internal temperature sensor temp vs V

Shutdown V = 1.79V



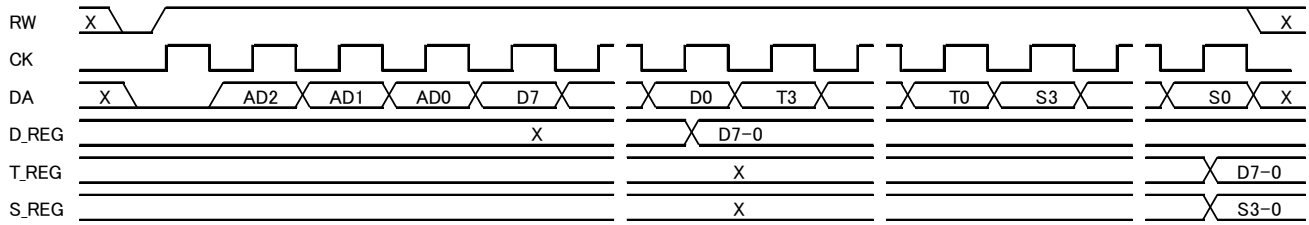
jeong.osc@gmail.com

SPI interface timing

Host MPU to P1 data write.

P1 send the data to host MPU.

Write timing



D7-0 : Dimming data(Write)

AD2_0 : Chip address data(0-7)

D_REG : dimming data(resistor output)

T_REG : test data(registor output) ; Select the test monitor output

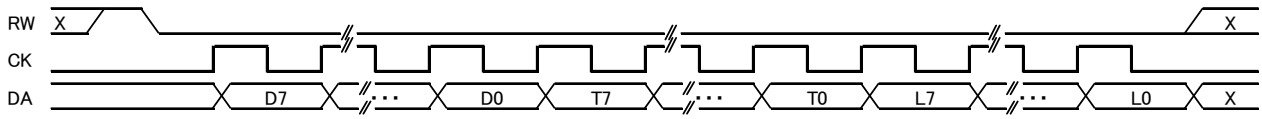
S_REG : test data(register output) ;

S<1>=0→ PS data enable S<1>=1→ Dimmer data change by register

S<3>=0→ Test output S<3>=1→ Test 2 output

P1 will be edge detection from CK and ignored first data.

Read timing



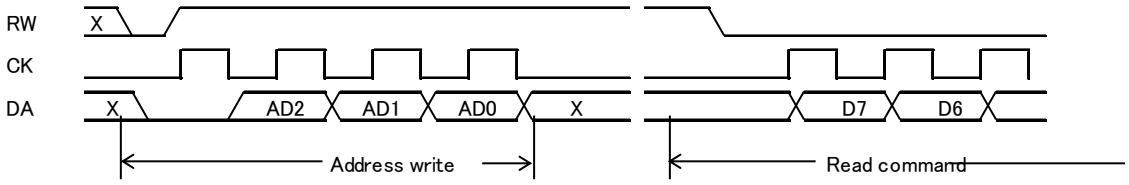
D7-0 : Dimming data(Read)

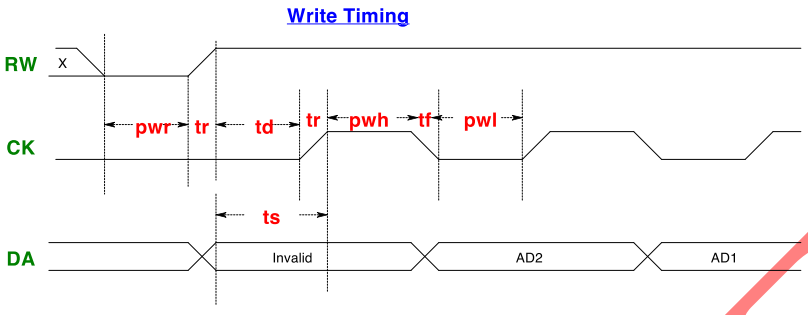
T7-0 : Temperature data

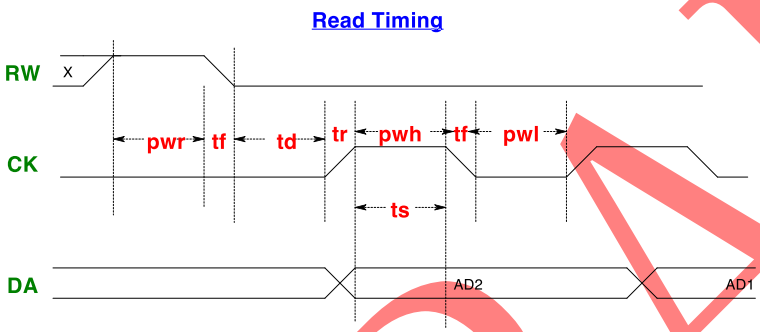
L7-0 : Photo diode ambient data

P1 can read edge rise of CK and MPU can edge down of CK read.

Read timing(address reserved)







Timing:

pwr: RW pulse width	; >10uS
tf: Fall time	; <100nS
td : Delay time	; >5uS
tr: Rise time	; <100nS
pwh; Clock High level	; >5uS
pwl; Clock low level	; > 5uS
ts; Read data point	; >5uS>pwh +2*ts

Detailed Description

The FIDES-P1 is a highly integrated, flexible, multi-string LED driver that uses external MOSFETs to allow high LED string currents, and includes temperature power supply control to maximize LED life efficiency. The driver optionally connects to a LED string faults fix-up functions help to black out of luminaire system.

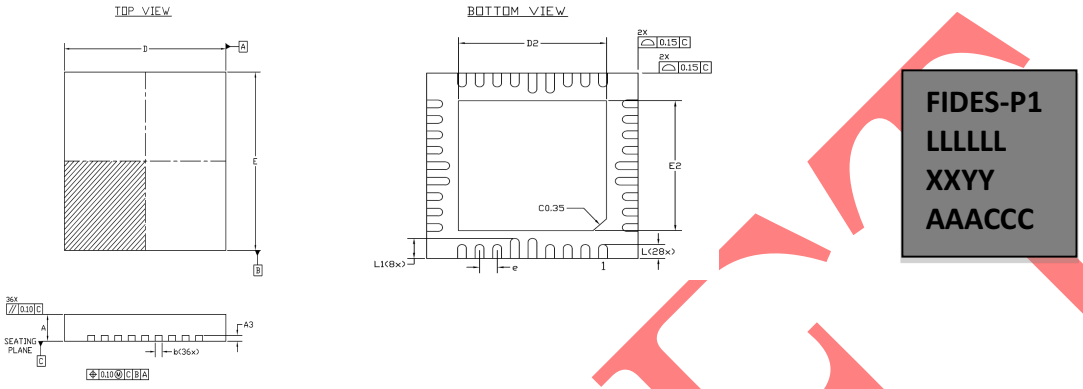
The easy install to plug in light sensor offer automatic dimming control for intelligent ECO power saving. Synchronization for use in FIDES SPI format to controlled LED TV backlight applications.

The drivers provide multiple methods of controlling LED brightness, through both peak current control and pulse width control of the PLC and light sensor, internal temperature drive signals. Peak temperature control offers excellent MTBF consistency, while pulse width control allows brightness management.

An on-chip temperature sensor is selectable variable register values. At over temperature, automatically shut-down or decrees power driving. All resister values are read and wright to changeable through the serial interface if a different power condition is desired.

QFN-36 Package Typical Pad Layout

QFN-36 Package Dimension

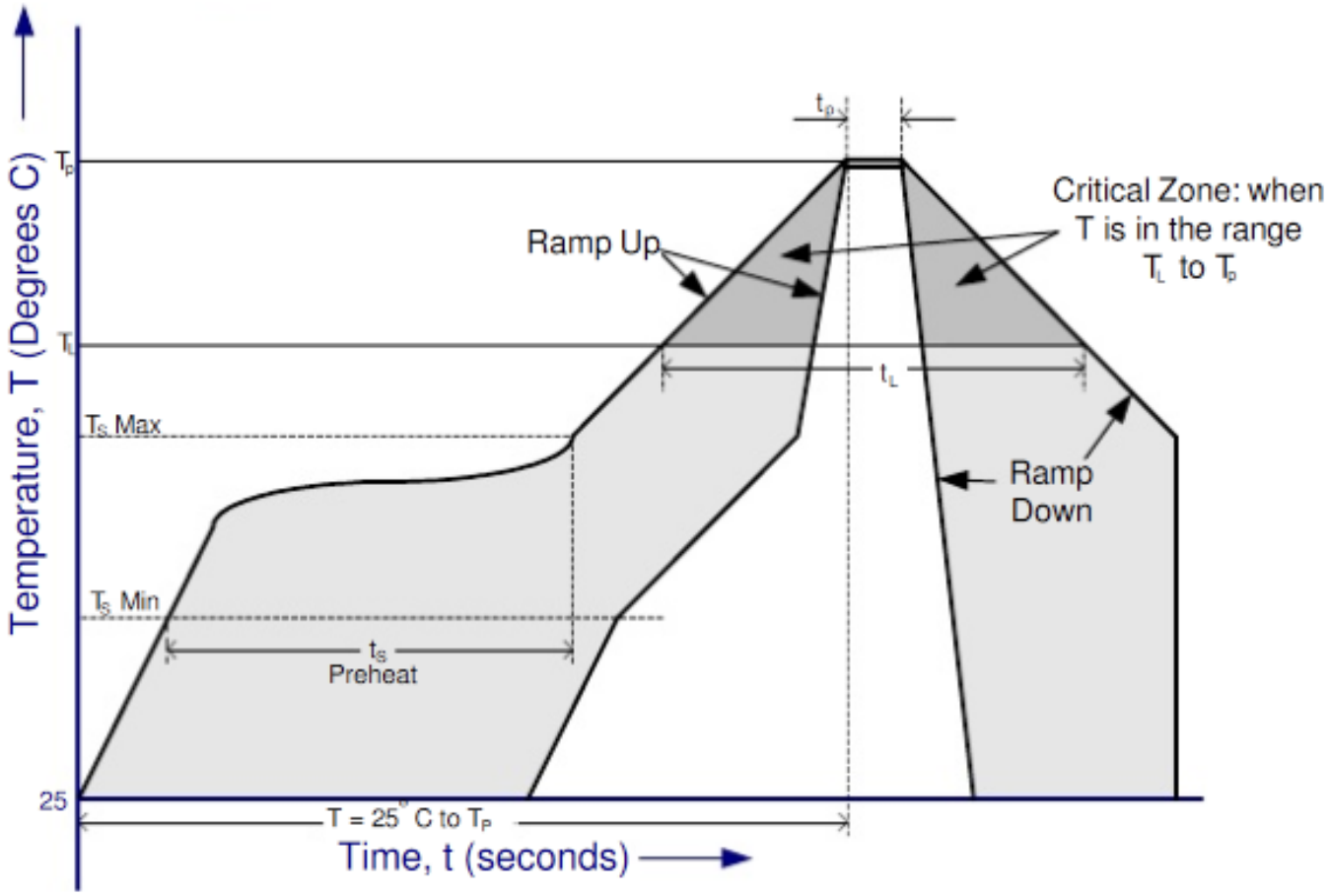


SYMBOL	COMMON					
	DIMENSIONS MILLIMETER			DIMENSIONS INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.85	0.90	0.95	0.034	0.036	0.038
A3	0.203 REF			0.008 REF		
b	0.20	0.25	0.30	0.008	0.010	0.012
D	5.85	6.00	6.15	0.230	0.236	0.242
D2	4.10	4.20	4.30	0.161	0.165	0.170
E	5.85	6.00	6.15	0.230	0.236	0.242
E2	4.10	4.20	4.30	0.161	0.165	0.170
e	0.500 BSC			0.020 BSC		
L	0.40	0.45	0.50	0.016	0.018	0.020
L1	0.60	0.65	0.70	0.024	0.026	0.028

The FIDES-P1 is supplied in a RoHS compliant leadless QFN-36 package. The package is lead (Pb) free, and used a 'green' compound. The package is fully compliant with European Union directive 2002/95/EC.
This package is 6mm x 6mm. The solder pads are on a 0.50mm pitch. The above mechanical drawing shows the QFN-36 package. All dimensions are in millimeters.
The center pad on the base of the FIDES-P1 is internally connected to AGND.
The date code format is XXYY where XX = two-digit week number, YY = two-digit year number.

jeong.osc@gmail.com

Solder Reflow Profile



The FIDES-P1 is supplied in Pb free QFN-36 package.
The recommended solder reflow profile for package options is show above.

jeong.osc@gmail.com

Table for Reflow Profile Parameter Values

The recommended values for the solder reflow profile are detailed in this table. Values are shown for both a complete Pb free solder process.

Profile Feature	Pb Free Solder Process	Non-Pb Free Solder Process
Average Ramp Up Rate (T_s to T_p)	3°C / second Max.	3°C / Second Max.
Preheat - Temperature Min (T_s Min.) - Temperature Max (T_s Max.) - Time (t_s Min to t_s Max)	 150°C 200°C 60 to 120 seconds	 100°C 150°C 60 to 120 seconds
Time Maintained Above Critical Temperature T_L: - Temperature (T_L) - Time (t_L)	 217°C 60 to 150 seconds	 183°C 60 to 150 seconds
Peak Temperature (T_p)	260°C	240°C
Time within 5°C of actual Peak Temperature (t_p)	20 to 40 seconds	20 to 40 seconds
Ramp Down Rate	6°C / second Max.	6°C / second Max.
Time for T= 25°C to Peak Temperature, T_p	8 minutes Max.	6 minutes Max.

FIDES makes no representations or warranties with respect to the accuracy or completeness of the contents of this document and reserves the right to make changes to specifications and products descriptions at any time without notice. FIDES does not make any commitment to update the information contained herein. Unless specifically provided otherwise, FIDES products are not suitable for, and shall not be used in, automotive applications. FIDES products are not intended, authorized, or warranted for use as components in applications intended to support or sustain life.

jeong.osc@gmail.com